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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,704	05/29/2001	Hiroyasu Ito	01-149	5746

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/865,704	ITO ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2001 and 01 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *15-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Claims 15 – 28 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5 filed on 02-01-02.

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement filed 05-29-01, entered as Paper No. 3

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claim 1 – 2*** *are rejected* under 35 U.S.C. 102(b) as being anticipated by Prior Art as admitted in Applicants' disclosure.

With regard to claim 1: Prior Art, for instance as explicitly admitted by Applicants in their disclosure (cf. page 2 of Specification and Fig. 22B), teaches

a semiconductor substrate 1 (cf. page 2, lines 12-13) having a principal surface of a first conductivity type (n-type);

a second conductivity type region 3 having island shape (cf. page 2, line 17), formed on the principal surface of said semiconductor substrate with a smooth concentration profile in a depth direction of the semiconductor substrate

(cf. Fig. 21), showing a smooth profile within the second conductivity region or base region 3;

a first conductivity type region 4 (cf. page 2, lines 21-22) inside said second conductivity type region, said first conductivity type inherently due to the introduction of impurities of the first conductivity type;

a trench 5 (cf. page 2, line 22) formed in the semiconductor substrate extending from a surface of said first conductivity type region so as to reach at least said second conductivity type region 3 on said first semiconductor substrate 1 (cf. Fig. 22B);

an insulation film 6 (cf. page 2, line 24) formed on an inner wall surface of said trench; and

an electrode portion made of polycrystalline silicon 7 (forming the gate electrode 8) (cf. page 2, line 26 – page 3, line 2) filled in said trench with said insulation film interposed there between (cf. Fig. 22B).

The stipulation within claim 1 that the aforementioned second conductivity type region is formed by introducing impurities of a second conductivity type by a plurality of ion implantation steps does not constitute a limitation on the device but instead pertains to a method of making said device. In keeping with the election by Applicants of the device claims 1-14 said stipulation is left out of consideration.

In conclusion, the Prior Art as disclosed by Applicants anticipates claim 1.

With regard to claim 2: the electrode portion of claim 1 as taught by the Prior Art as disclosed by Applicants in Fig. 22B is formed to have a T-shaped cross section composed of a first part filling the trench and the second part protruding on the principal surface of the semiconductor substrate (cf. Fig. 22B, particularly the T shape of the region with numeral 8).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claims 3 – 5*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over the Prior Art as disclosed by Applicants (cf. pages 2-3 of the Specification) in view of Huang (6,110,799).

Prior Art, for instance as explicitly admitted by Applicants in their disclosure (cf. page 2 of Specification and Fig. 22B), teaches

a semiconductor substrate 1 (cf. page 2, lines 12-13) having a principal surface of a first conductivity type (n-type);

a second conductivity type region 3 formed on the principal surface of said semiconductor substrate having island shape (cf. page 2, line 17);

a highly doped first conductivity type region 4 (cf. page 2, lines 21-22) formed inside said second conductivity type region, said first conductivity type inherently due to the introduction of impurities of the first conductivity type at high concentration;

a plurality of trenches or first trenches 5 (cf. page 2, line 22) each extending from a surface of said highly doped first conductivity type region so as to reach at least said second conductivity type region on said first semiconductor substrate (cf. Fig. 22B);

an insulation film 6 (cf. page 2, line 24) formed on an inner wall surface of each of the first trenches; and

an electrode portion made of polycrystalline silicon 7 (forming the gate electrode 8) (cf. page 2, line 26 – page 3, line 2) filled in each of the first trenches with said insulation film interposed there between (cf. Fig. 22B).

The Prior Art as disclosed by Applicants does not necessarily teach a plurality of second trenches and a second conductivity type protrusion region as stipulated in Applicants' claim 3.

However, for the specific purpose of protecting the gate trenches against breakdown, Huang (cf. Fig. 9) teaches a semiconductor device with trenches (cf. abstract, first sentence) comprising a plurality of first trenches with an electrode portion 26 made of polysilicon (cf. column 2, line 24) and insulation layer 24 (cf. column 2, line 15) similar to Applicants' first trenches, and also comprising a plurality of second trenches 34 (cf. Fig. 8 and column 3, line 39; see also column 2, lines 32 and 42) (the plurality of which is

implied by the function of said second trenches as structures to be placed in between adjacent members of the said plurality of first trenches, said latter plurality being inclusive of the possibility of more than two first trenches) formed inside the second conductivity type region 14 (cf. column 2,line 5) so that each of the second trenches is positioned between an adjacent pair of said first trenches in parallel with said first trenches (cf. Fig. 9), such that a second conductivity type (P type) protrusion region 35 (cf. Fig. 9 and column 2, lines 41-42) is formed with a junction deeper than the junction of said second conductivity type region (cf. column 3, lines 1-4) and in electrical contact with the highly doped first conductivity type region 14. It is inherent in impurities in semiconductor material that they must have been introduced while, because of the election by Applicants of the device invention, as opposed to a method of making invention, the manner in which said impurities may be introduced is irrelevant to the present examination of the invention. *The aforementioned purpose for including the second trenches and protrusion,* namely the protection against breakdown of the trench gates, *is obviously useful in the specific case* of the plurality of first trenches admitted to be prior art by Applicants.

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as taught by the prior art as admitted by Applicants at the time it was made so as to include the further limitations involving the definitions of said plurality of second trenches and said second conductivity type protrusion region.

With regard to claim 4: the Prior Art as admitted by Applicants teaches the said electrode portion to have a T shaped cross section composed of a first part filling the

trench and a second part protruding on the principal surface of the substrate (cf. Fig. 22B). Therefore, claim 4 does not distinguish over the prior art.

With regard to claim 5: although the Prior Art as admitted by Applicants do not necessarily teach the further limitation as defined by claim 5, Huang teaches an electrode 36 (cf. column 2, lines 39-43) connecting said highly doped first conductivity type region 16 (cf. Fig. 9) to said second conductivity type protrusion region 35 through said second trench, said contact being essential in aforementioned protection function of the plurality of second trenches, as explained above in the discussion of claim 3. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by claim 3 at the time it was made so as to include the further limitation of claim 5.

5. ***Claims 6 - 10*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted by Applicants and over Huang as applied to claim 3 above, and further in view of Yu et al (6,213,869 B1). As detailed above, claim 3 is unpatentable over Prior Art as admitted by Applicants in view of Huang.

Although neither the Prior Art as admitted by Applicants nor Huang teach the further limitation as defined by claim 6, it is known in the art as witnessed by Yu et al (cf. abstract, second sentence, and column 1, lines 7-15) that a floating body region creates a capacitor between body region and gate in MOSFET devices, resulting in a higher threshold voltage when the MOSFET is OFF than when it is ON, thus reducing steady state power dissipation. To combine this feature with the trench power MOSFET casu

quo IGBT of Applicants is *obvious* because the higher withstand voltage aimed at needs to be achieved at reasonable costs with regard to power dissipation in the ON state. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by claim 3 at the time it was made so as to include the further limitation of claim 6.

With regard to claim 7: Huang teaches a first electrode provided in one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity region through one of the second trenches, while the plural nature of said second trenches is implied by their positioning in between the first trenches given the plural nature of said first trenches, comprising the case of more than two; hence Huang also teaches a second electrode provided in another one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity type region through the other one of said second trenches, the second electrode being disposed adjacent to the first electrode.

Although neither Prior Art as disclosed by Applicants nor Huang necessarily teach one of said adjacent pair of first and second electrodes to be in a floating state, said floating state would add the said type conductivity protrusion region to the floating body region for the well-defined *purpose* of enhancing the effect of the capacitor formed between the gate and the thus extended body region, thereby adding to the difference between the threshold voltages in the OFF, respectively ON states, and thus further

improving the possibility to combine high OFF state threshold voltage with low power dissipation in the steady state operating mode of the device.

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention defined by claim 3 at the time it was made so as to include the further limitation of claim 7.

With regard to claim 8: the second conductivity type protrusion region 35 is itself a highly doped region, and therefore can be thought of as split into two sub-regions, a first part, consisting of a highly doped region contacting said electrode 36 and disposed between said electrode and the remaining (second) part of said second type protrusion region 35. Therefore, the further limitation of claim 8 does not distinguish over the prior art.

With regard to claim 9: in the Prior Art as admitted by Applicants (at least) one of said plurality of first trenches encloses the second conductivity type region entirely (cf. Fig. 22B). Therefore, the further limitation as defined by claim 9 does not distinguish over the prior art.

With regard to claim 10: Huang teaches the first trenches to be shallower than the second conductivity type protrusion regions (cf. column 3, lines 1-4) for the purpose of trench gate protection. Since each trench gate needs protection it would have been obvious to teach the further limitation of claim 10.

6. ***Claims 11 – 14*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted by Applicants in their disclosure (pages 2-3 and Fig. 22B) in view

of So et al (5,895,951). As detailed above, Prior Art as admitted by Applicants anticipates claim 1.

Said Prior Art does not necessarily teach the further limitation as it is defined by claim 11.

However, the inclusion of a plurality of electric field alleviating regions formed by introducing impurities of the second conductivity type in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region has long been known in the art of trench MOSFET structures, as evidenced by So et al, who teach deep-P regions 116 (cf. column 4, line 9-11, and Fig. 2) annex doping trenches 112 *for the specific purpose* of suppressing incidental turn-on of parasitic bipolar transistor function (cf. column 3, lines 33-42). Said regions 116 surround the body region, enclosing a peripheral portion of it. Moreover, said regions are composed of a strip-wise third trench 112 (cf. column 4, line 4) and second conductivity type deep-P regions 116 in which impurities of the second conductivity type have been introduced in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region, whilst the pn junction of the electric field alleviating regions is deeper than a pn junction of aforementioned second conductivity type region (cf. column 3, lines 33-50 and Fig. 2). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by claims 11 – 13.

With regard to claim 14: the further limitation as defined by claim 14 does not add anything to the device specifications and is merely a statement of obvious use. Vertical trench MOSFET devices such as defined by claim 11 have long been known by people

of ordinary skills to be useful as gate driving power elements for controlling the conduction state between the back surface of their semiconductor substrate and their source (first conductivity type region in the present invention and claims) by using said electrode portion (comprising gate) as a control electrode. Therefore, the further limitation of claim 14 is moot as device limitation, and does not distinguish Applicants' invention over the prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
February 18, 2002